AMENDMENT TO SPECIFICATION

IN THE SPECIFICATION:

A marked-up copy of the changes to selected paragraph(s) is provided below. Please enter these changes to the specification in the record.

Please replace the paragraph that begins at line 9 of page 5 with the following paragraph:

Figures 2(a) through 2(j) illustrate an exemplary process for forming a n[[p]]-type transistor according to the invention;

Please replace the paragraph that begins at line 11 of page 5 with the following paragraph:

Figures 3(a) through 3(d) illustrate an exemplary process for forming a p[[n]]-type transistor according to the invention;

Please replace the paragraph that begins at line 15 of page 11 with the following paragraph:

Patterned photoresist layers (not shown), which are removed prior to the next stage of the process, are used to successively create the source/drain regions of the transistors. For the n-type transistors, a shallow and high-dose of arsenic ions, for example, may be used to form the source/drain regions 240 and 241 while the p-type transistors are covered with the corresponding photoresist layer. As discussed above, in the methods according to this invention, the source and drain regions 240 and 241

are formed in upper portions of semiconductor substrate 200 (i.e., not removed and reformed). For the p-type transistors, (discussed below with regards to Figures 3(a) – 3(d)), a shallow and high dose of BF_2 ions, for example, may be used to form the source/drain regions [[30]] 340 and 341 while the n-type transistors are covered with the corresponding photoresist layer. An anneal is then used to activate the implants. The exposed oxide on the structure is then stripped by dipping the structure in HF in order to expose bare silicon in the source, gate and drain regions of the transistors.

Please replace the paragraph that begins at line 22 of page 13 with the following paragraph:

Figure 4 depicts a top-down view of a transistor according to the invention. A cross-sectional view taken along line A-A of Figure 4 is the structure shown in Figure 2(i) and a cross-sectional view taken along line B-B of Figure 4 is the structure shown in Figure 2(j). As shown in Figure 4, the gate electrode [[242]] 237 with the spacer 238 is located above the semiconductor substrate 200. The oxide fill 233 (i.e., shallow trench isolation structure) isolates the source and drain regions 240 and 241 of the semiconductor substrate 200.